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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,877	07/29/2003	Mahmoud K. Jibbe	03-0272	5581

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EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 10/629,877	**Applicant(s)** JIBBE, MAHMOUD K.	
	Examiner Duc T. Doan	**Art Unit** 2188	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 19 October 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1-12 and 14-27*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER

Continuation of 11. does NOT place the application in condition for allowance because:
Response to Arguments
Applicant's arguments in response to the last office action has been fully considered but they are not persuasive. Examiner respectfully traverses Applicant's arguments for the following reasons:
Per the remarks on pages 7-11 for claim 1,
A) Applicant argues that Sawdy does not teach the two storage controller modules (specification's Fig 1: #70), wherein each storage module contains two storage array controller units (specification's Fig 1: #72). Examiner respectfully disagrees. Sawdy discloses two storage controller modules (Sawdy's Fig 2: controller A module, controller B module); each storage controller module contains two storage array controller units (Sawdy's Fig 2: I Port 0, Port 1 storage controller units of controller A module).
Applicant argues that Sawdy does not disclose the two controllers do not function as a primary and a redundant backup. Sawdy's column 1 lines 7-30 clearly discloses the two controllers can access the same group of disk drives in a redundancy manner (Sawdy's column 1 lines 7-10), when there is a failure, the control can be switched smoothly to the backup controller (Sawdy's column 1 lines 25-30). Sawdy further discloses the two controllers can access the same group of disk array as shown in Sawdy's Fig 4: #404. Examiner thanks Applicant for pointing out a typographic error in previous action, that is "Fig 5: 70" is wrongly typed, it should be typed as "Sawdy's Fig 4: #404".
B) Rausner's column 2 lines 56-68 teaches the two controllers, using a link between controllers, sometimes called a heartbeat connect which is used to inform each other the status of the other controller. Should one controller fail to send or response to a signal, the other controller initiates failover activity. Thus Rausner clearly discloses the first controller sends out a signal (corresponding to the claim's the first storage array controller module provides an availability signal to the second storage array controller module), and if the second controller does not receive this signal during a period of time, it detects the first controller fail to send, (corresponding to the claim's the second storage array controller module dose not receive a signal from the fist storage array controller module within a given time period), the second controller initiates/executes fail over activity, taking over the failed first controller (corresponding to the claim's the second storage array controller module asserts control over the array of storage devices).

Thus Rausner clearly describes the Examiner previous statement that is, the heartbeat is sent periodically from one controller to the other to inform each other the status of the other controller. Such that if the receiving/second controller does not receive this signal sent from the first controller within a time period, the receiving/second controller detects the first controller fail to send and the second controller initiates/executes fail over activity.

C) Applicant's remark on page 9, second paragraph 9 of heartbeat problem. Examiner notes that Applicant does not clearly states what is the problem of heartbeat. Applicant's agues "Rauscher is concerned with double cabling to proof a RAID system against any single point of failure, not utilization of a heartbeat signal". Applicant then leaps to conclusion "..would not motivate others to operate with a heartbeat signal". Examiner challenges Applicant to point out the page and lines in Rauscher that states "not utilization of a heartbeat signal". Rauscher clearly teaches using heartbeat signal as discussed in item B. In fact, Rauscher further teaches any critical components should have dual redundancy components, for example dual redundancy of raid controllers (Rausner's column 2, lines 20-25), disks media, disk channels, disk channel controller chips (Rausner's column 2 lines 35-47), cables, connectors, terminators, boards, cooling, power supplies should have redundancy (Rausner's column 3 lines 1-15). By providing redundant components, if one component fails, the other still operates, thus the operation of the system will not be interrupting (Rausner's column 3 lines 14-16).

Examiner notes that both Sawdy and Rausner teach innovations to provide the advantage of using redundant components in a storage system such that if one fails, the operation of the overall system can still operate with the remaining component.
D) Regarding the remarks on page 10, The first and second array controller units within a storage array controller module is disclosed in Sawdy's Fig 3, and discussed in item A. Examiner does not rely on Cruynigen to teach the above limitation. However, Cryuningen discloses a method in which the storage array controller modules (Cryuningen's Fig 7: #20a, #20d storage array modules) work in conjunction with the array controller units (Cryuningen's Fig 7: storage channels 14ad1, 14ab2, 14cd2) to control arrays of storage devices (disks in a storage array 20a, 20d). Cryuningen discloses disks in the storage arrays can be easily reconfigured/grouped so that they can be accessed by both storage array controller modules or in separate groups of devices so that a group of device only accessed by a particular storage array controller module (Cryuningen's paragraph 40). By providing a method of easily grouping disks such that any storage array controller module has the capability of accessing every storage device seamlessly (Cryunigen's paragraph 37). One skill in the art would be motivated to include Cryuningen's method and apparatus into Sawdy's system so that in case one controller has failed, the surviving controller has access to all the storage devices seamlessly (Cryuningen's paragraph 38). . One skill in the art would be motivated to apply Cryuningen's teaching to add more disks into the system (Cryuningen's paragraph 42) so that the disk capacity and performance of the system can be scaled up easily (Cryiningen's paragraph 36).
E) Regarding Applicant's remarks on page 11 for claim 3, the claim is rejected based on the rational as discussed in above paragraphs.
F) Regarding Applicant's remarks on page 12 for claims 5-7, the claim is rejected based on the rational as discussed in above paragraphs.
G) Regarding Applicant's remarks on pages 12-15 for claims 10-12,14-18,20,22-27, Applicant argues that Workman does not disclose the handshake protocol that requires the first controller/node sending out a signal and the second controller/node sends a response signal. Workman's paragraph 30 lines 12-14 discloses the first storage controller/node monitors the heart beat path (Fig 1: #74) and determines if the second storage controller/node operation normally. Workman's paragraph 31 lines 11 to 15 discloses the first storage controller/node sends a signal to the second storage controller/node (a token), the second storage controller/node does not response, or incorrectly response, the first controller/node will detect that the second node fails. Therefore, Workman clearly discloses the heartbeat mechanism represents the handshake protocol.
H) Regarding Applicant's remarks on pages 13-15 for claim 10, Applicant argues, "Jain does not disclose separate queues at all". Examiner respectfully disagrees. Jantz describes each intelligent storage controller (Fig 3: RDAC) having its own queue (Fig 3: #306, #308), the queue is in each embedded storage controller module within the storage subsystem (see Jaint's column 1 lines 40-45), the queue is used to stored the I/O requests for the desired I/O path (Jain's column 2 lines 4-10), if one of the storage controller fails, the remaining storage controller can take over operation using multiple redundant paths (Jain's column 1 lines43-47). Jain further discloses

I/O requests can be send to any prefer paths of the redundant I/O paths via multiple storage controllers being operated in redundant active controllers (see Jain's column 1 lines 45-60).
I) Regarding Applicant's remarks on page 15 for claims 22-27, the claim rejected based on the same rationale as discussed in item H.
J) Regarding Applicant's remarks on page 15 for claims 19,21, the claims rejected based on the same rationale as of claim 10,

storage array controller (specification's Fig 1: #70; paragraph of the instant application each contain two controller units.
Examiner respectfully disagrees.
1) Beardsley's column 1, lines 28-38 describes the advantage of caching data in multiple levels of memory (including semiconductor memories) by optimizing the differences in each level's access time (i.e accessing data in small capacity cache at higher level is faster than accessing data in large capacity memory at lower level). In a similar manner, Ignatowski's Fig 1,2 shows a topology in which data in caches (Ignatowski's Fig 1: #2 cache) are switched to memory (Ignatowski's Fig 1: #5 memory, column 1 lines 15-40). Since the higher cache memory has quicker access time than the lower cache memory, the data obtain from the higher cache memory will be returned to the host faster that getting data from the lower cache memory. Therefore, it's obviously to include the cache and main memory structures as showed in Ignatowksi's Figs 1 and 2 in Beardsley's system thereby allowing to optimize the access of data in a hierarchical memory configuration that are shared by multiple processors (Ignatowski's column 1 lines 59-67). Examiner notes that specification page 20 explains the same rationale as mentioned above. Beardsley's Fig 3 and 4 clearly show the ports of switching circuits that allow processors and DASD devices interconnecting to the cache and main memory.
2) As per the remarks on pages 9-10 for claims 3-5, they are rejected based on the same rationale as in above paragraphs. Ignatowski's Figs 1 and 2 clearly shows "the bus that connecting two or more processors and the cache memory and for allowing the faster data transmission than that of the connection network.." as recited in claim 4. Furthermore, Beardsley clearly describes the storage controller (Fig 3: #325) includes dual clusters (Fig 3: #360,361), each cluster having separate power supply, therefore they are clearly must be in separated packages with separate power supplies. (Beardsley's column 11, lines 8-12). Beardsley further describes the cache can be accessed by both clusters (Beardsley's column 11, lines 10-32).
3) As per the remarks on page 10 for claim 10, Examiner respectfully disagree, any memory such as cache memory are capable of storing any data that are accessed in random or in sequential access manner. Ofek's column 2 line 30 to column 3 line 21 clearly describes the method that organizes cache to store data in two areas for demand fetching from host (i.e data being accessed in a random manner) and prefetching data (i.e data being accessed in a sequential manner)..